

REMARKS

Claims 1-31 and 99 are pending in the present application.

Claims 1-3, 7-16, 18-25, 29-31 and 99 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,338,996 ("Iizuka"). Applicants respectfully traverse this rejection.

Claim 1 recites a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized gas *annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with a *second annealing process*," as recited in claim 1 (emphasis added).

Iizuka discloses "a semiconductor memory device production method for a semiconductor memory device having a capacitor formed by a high dielectric insulation film and a noble metal upper electrode which are successively layered on a noble metal lower electrode, the method being characterized in that the formation of the capacitor is followed by anneal in a nitrogen atmosphere of 1 atmospheric pressure at temperature of 300 to 400 degrees C" and a "semiconductor memory device production method for a semiconductor memory device having a capacitor formed by a high dielectric insulation film and a noble metal upper electrode which are successively layered on a noble metal lower electrode, the method being characterized in that the formation of the capacitor is followed by anneal in a gas mixture atmosphere of oxygen concentration of 5% or below and nitrogen under 1 atmospheric pressure at temperature of 300 to 400 degrees C." (Iizuka, Summary of the invention)

Contrary to the suggestion in the Office Action, Iizuka does not disclose all the limitations of claim 1. Iizuka does *not* disclose an *annealed* dielectric layer *and* a separately annealed top conducting layer. The final structure in Iizuka is different from the claimed invention as a result of using only a single anneal process.

Contrary to the suggestion in the Office Action, this is not a question of product by process, but a question of whether the device disclosed by Iizuka anticipates the claimed invention. Since Iizuka does not disclose all the limitations of claim 1, claim 1 and claims 2-3, 7-16, 18-25 and 29-31 depending therefrom are patentable over Iizuka. Claim 99 recites similar limitations to claim 1, including, *inter alia*, "an annealed dielectric layer . . . that has been annealed with a first oxidizing gas anneal process; and an upper electrode . . . which is an oxidized gas annealed layer formed over said annealed dielectric layer that has been annealed with a second oxidizing gas anneal process." For at least the same reasons as discussed with respect to claim 1, claim 99 is patentable over Iizuka. Accordingly, Applicants respectfully request that the 35 U.S.C. § 102(e) rejection of claims 1-3, 7-16, 18-25, 29-31 and 99 be withdrawn.

Claims 4, 5 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh"). Applicants respectfully traverse this rejection.

Claims 4, 5 and 17 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits.

As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode

consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed* dielectric layer, wherein said annealed top conducting layer is annealed with *a second annealing process*," as recited in claim 1 (emphasis added).

Emesh does not cure the deficiency of Iizuka in this respect. The Office Action asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the bottom electrode of Iizuka with the metal alloy or conductive metal oxide material, as taught by Emesh, so as to provide an alternative material to make the bottom electrode." However, Iizuka *teaches away* from this combination. Iizuka discloses a "semiconductor device having a capacitor formed by a high dielectric insulation film and a *noble metal* upper electrode which are successively layered on a *noble metal* lower electrode." Col. 2, lines 28-31; Col. 2, lines 38-40. (Emphasis added). Iizuka specifically discloses that "[t]he lower electrode 28 *and* the upper electrode 28 are formed by a *noble metal film* such as Ru, Ir, and Pt." Col. 3, lines 38-40. (Emphasis added).

Since Iizuka teaches that *both* electrodes in the capacitor should consist of a *noble metal*, Iizuka teaches away from Emesh's metal alloy or conducting metal oxide for either the upper or lower electrodes in Iizuka and there is no motivation to combine the teachings of Iizuka and Emesh.

Since the cited references do not teach or suggest all the limitations of claim 1, claims 4, 5 and 17 depending therefrom are patentable over the reference. Furthermore, the Office has not identified any motivation in either Emesh or Iizuka to overcome their divergent teachings to achieve the claimed invention. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 4, 5 and 17 be withdrawn.

Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers"). Applicants respectfully traverse this rejection.

Claims 6 and 14 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed dielectric layer*, wherein said annealed top conducting layer is annealed with a *second annealing process*," as recited in claim 1 (emphasis added).

Alers discloses "a method of forming a capacitor in a semiconductor wafer having a plurality of stacked layers including a substrate, a first dielectric layer including a via that extends through the first dielectric layer and contacts the substrate. The semiconductor wafer also includes a second dielectric layer having a tungsten plug that extends through the second dielectric and contacts the via and that forms a bottom electrode of the capacitor. The method of the present invention comprises a first step of removing a part of the second substrate around the plug to expose a surface thereof. The exposed surface of the plug is then nitridized to form Tungsten Nitride (WN) or Titanium Nitride (TiN) and a capacitor dielectric is formed from a metal oxide material deposited over the nitridized surface of the plug. Alternatively, a metal-nitride is deposited over the tungsten plug to form the bottom capacitor plate. The capacitor dielectric is then annealed and a top electrode of the capacitor is formed over the capacitor dielectric." (Alers, Summary of the invention)

Alers does not cure the deficiency of Iizuka in this respect. The Office Action asserts that "it would have been obvious to one of ordinary skill in the art . . . to modify the invention of Iizuka with the bottom electrode made of metal nitride, as taught by Alers, so as to provide an alternative material for the bottom electrode." However, as noted above, Iizuka *teaches away* from this combination. As such, Alers cannot be combined with Iizuka since Iizuka teaches away from any material other than noble metals for a bottom electrode. Accordingly, the references do not teach or suggest all the limitations of claim 1 and claims 6 and 14 depending therefrom, and Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 6 and 14 be withdrawn.

Claims 26 and 27 stand rejected under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar"). Applicants respectfully traverse this rejection.

Claims 26 and 27 depend from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed dielectric layer*, wherein said annealed top conducting layer is annealed with a *second annealing process*," as recited in claim 1 (emphasis added).

Narkwankar discloses "A capacitor structure comprising a bottom electrode, an insulator and a top electrode, and method for manufacturing the same. The bottom and top electrodes preferably include a metal portion and a conducting oxygen-containing metal portion. In one embodiment, a layer of ruthenium is deposited

to form a portion of the bottom electrode. Prior to deposition of the insulator, the ruthenium is annealed in an oxygen-containing environment. The insulator is then deposited on the oxygen-containing ruthenium layer. Formation of the top electrode includes depositing a first metal on the insulator, annealing the first metal and then depositing a second metal. The first and second metals may be ruthenium.”

(Narkwankar, Abstract)

Narwankar does not overcome the deficiencies of Iizuka. Narwankar discloses a plasma enhanced annealed layer, but does not disclose “an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed dielectric layer*, wherein said annealed top conducting layer is annealed with a *second annealing process*,” as recited in claim 1. Since Iizuka and Narwankar, neither separately or in combination, do not teach or suggest all the limitations of claim 1, claims 26 and 27 depending therefrom are patentable over the reference. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 26 and 27 be withdrawn.

Claim 28 stands rejected under 35 U.S.C. § 102(e) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,387,802 (“Marsh”). Applicants respectfully traverse this rejection.

At the outset, Marsh has a filing date of June 15, 2000, which is *after* the filing date of the present application. Thus, the subject matter of Marsh does not qualify as prior art. This has not been addressed by the Office in its response to “Response to Arguments” discussion. This reference cannot be applied against the claimed invention as a primary reference or as a secondary reference to cure a deficiency of a primary reference.

Furthermore, claim 28 depends from claim 1 and should be similarly allowable with claim 1 for at least the reasons provided above with regard to claim 1, and on their own merits. As discussed above, Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed dielectric layer*, wherein said annealed top conducting layer is annealed with a *second annealing process*," as recited in claim 1 (emphasis added). Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claim 28 be withdrawn.

Marsh discloses "A method of depositing a platinum based metal film by CVD deposition includes bubbling a non-reactive gas through an organic platinum based metal precursor to facilitate transport of precursor vapor to the chamber. The platinum based film is deposited onto a non-silicon bearing substrate in a CVD deposition chamber in the presence of ultraviolet light at a predetermined temperature and under a predetermined pressure. The film is then annealed in an oxygen atmosphere at a sufficiently low temperature to avoid oxidation of substrate. The resulting film is free of silicide and consistently smooth and has good step coverage."
(Marsh, Abstract)

Marsh also fails to cure the inadequacies of Iizuka and fails to disclose Iizuka does not teach or suggest a capacitor comprising, *inter alia*, "a bottom conducting layer . . . an *annealed dielectric layer*, wherein said annealed dielectric layer is annealed with a *first annealing process* . . . and a top electrode consisting of a single oxidized *gas annealed top conducting layer* formed over said *annealed dielectric layer*, wherein said annealed

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top conducting layer is annealed with *a second annealing process,*" as recited in claim 1 (emphasis added).

Nor has there been provided in the references, the motivation or ability to combine the references to achieve the claimed invention. As such, the rejection of claim 28 should be withdrawn and the claim allowed.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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